

**Amendments to the Specification:**

On page 1, please amend paragraph [0001] as follows:

[0001] The present application is related to U.S. Patent Application Serial No. 10/689,336 [[\_\_\_\_]] entitled "Method for Load Balancing a Loop of Parallel Processing Elements" filed [[\_\_\_\_]] (~~DB001068-000, Micon no. 02-1298~~) 20 October 2003, U.S. Patent Application Serial No. 10/689,355 [[\_\_\_\_]] entitled "Method for Using Filtering to Load Balance a Loop of Parallel Processing Elements" filed [[\_\_\_\_]] (~~DB001061-000, Micon no. 02-1296~~) 20 October 2003, U.S. Patent Application Serial No. 10/689,345 [[\_\_\_\_]] entitled "Method for Load Balancing a Line of Parallel Processing Elements" filed [[\_\_\_\_]] (~~DB001066-000, Micon no. 02-1267~~) 20 October 2003, U.S. Patent Application Serial No. 10/689,312 [[\_\_\_\_]] entitled "Method for Using Extrema to Load Balance a Loop of Parallel Processing Elements" filed [[\_\_\_\_]] (~~DB001067-000, Micon no. 02-1297~~) 20 October 2003, U.S. Patent Application Serial No. 10/689,365 [[\_\_\_\_]] entitled "Method for Load Balancing an N-Dimensional Array of Parallel Processing Elements" filed [[\_\_\_\_]] (~~DB001062-000, Micon no. 02-1295~~) 20 October 2003, and U.S. Patent Application Serial No. 10/689,382 [[\_\_\_\_]] entitled "Method for Rounding Values for a Plurality of Parallel Processing Elements" filed [[\_\_\_\_]] (~~DB001064-000, Micon no. 02-1269~~) 20 October 2003.

On page 8, please amend paragraph [0040] as follows:

[0040] In the current embodiment, the H-registers 42 are comprised of synchronous SRAM and each processing element within the processing element array 28 contains eight H-registers 42 so that two pages can be stored from different DRAM locations, thus allowing the interleaving of short i/o bursts to be more efficient. Result register pipeline 40 is also connected to one or more neighborhood connection registers ("X-register") (not shown). The X-register links one PE 30 to its neighboring PE's 30 in the processing element array 28. The reader desiring more information about the hardware shown in FIGs. 1 and 2 is directed to UK Patent application No. 0221563.0 (~~serial no. not yet assigned~~) entitled "Control of Processing Elements in Parallel Processors" filed 17 September 2002, (~~Micon no. 02-1604~~) which is hereby incorporated by reference.